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Filing Date	November 6, 2001
First Named Inventor	Mohammad A. Abdallah
Art Unit	2359
Examiner Name	Richard L. Ellis
Attorney Docket Number	42390P5943C

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
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- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
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- ☐ Proprietary Information
- ☐ Status Letter
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Remarks

Request for Rehearing under 37 CFR § 41.52

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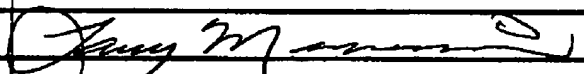
Signature			
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Docket No.: 42390P5943C

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:
Mohammad A. Abdallah et al.

Application No. 10/005,728

Filed: November 26, 2001

For: METHOD AND APPARATUS FOR COMPUTING A PACKED SUM OF ABSOLUTE DIFFERENCES

Examiner: Richard Ellis

Art Unit: 2183

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REQUEST FOR REHEARING UNDER 37 C.F.R. § 41.52

Mail Stop Appeal Brief-Patents
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Dear Sir:

Responsive to the Decision on Appeal of June 13, 2006, appellants submit the following brief in support of a Request for Rehearing pursuant to 37 C.F.R. § 41.52(a) for consideration by the Board of Appeals and Interferences.

TABLE OF CONTENTS

I. Status of the Claims (independent claims shown in bold)

Claims 1-7, 8-15, 19-20, 25, 32 and 38 are canceled.

Non-final rejection of claims 16-18, 21-22, 23-24, 26-31, 33-37 and 39-44 was appealed. A Decision on Appeal No. 2006-1169 was issued June 13, 2006.

Rejection of claims 17, 26-31 and 33-37 under 35 USC § 112, second paragraph, as allegedly being indefinite was sustained.

Rejection of claims 16-18, 26-31, 35-37 and 39-42 under 35 USC § 103(a) as allegedly being unpatentable over US Patent 5,859,789 (Sidwell) in view of in view of Visual Instruction Set (VIS ™) User's Guide, Sun Microsystems, March 1997 (Sun) was not sustained.

Rejection of claims 21-22, 23-24, 33-34 and 43-44 under 35 USC § 103(a) as allegedly being unpatentable over US Patent 5,859,789 (Sidwell) in view of in view of Visual Instruction Set (VIS ™) User's Guide, Sun Microsystems, March 1997 (Sun) and further in view of US Patent 5,721,697 (Lee) was not sustained.

A rehearing is being requested with regard the sustained rejection of claims 17, 26-31 and 33-37 under 35 USC § 112, second paragraph, for allegedly being indefinite.

II. Status of Amendments

A preliminary amendment, submitted by appellant on 11/6/2001 was entered. An official response to a first Office Action mailed 8/19/2003 was submitted by appellant on 1/20/2004 and was entered. A Final Office Action was mailed on 4/9/2004. Appellant responded with an amendment and official response after final on 6/9/2004, which was not entered. An Advisory Action was mailed 7/9/2004. An RCE and official response, which was not accepted, were submitted by appellant on 10/11/2004. A Notice of Non-Compliant Amendment was mailed 10/25/2004. Appellant responded by submitting a corrected official response on 11/5/2004, which was not accepted. A second Notice of Non-Compliant Amendment was mailed 12/9/2004. Appellant submitted a second corrected official response on 12/20/2004, which was entered. A Non-final Office Action was mailed on 1/10/2005. A Notice of Appeal was transmitted on 6/10/2005, and an appeal ensued. Another amendment was submitted, under 37 CFR § 41.33 and concurrent with the Appeal Brief.

Accordingly, the claims stand as of the amendment of 8/10/2005, and are reproduced in clean form in the Claims Appendix of the Rehearing Request.

III. Grounds of Rejection to be Reviewed on Rehearing

A. Claims 17, 26-31 and 33-37 stand rejected under 35 USC § 112, as allegedly being indefinite.

B. The Board summarily reversed the rejection of claims 17, 26-31, and 33-37 under 35 USC § 103(a). The Board indicated that their technical reversal did not imply that the art relied upon by the Examiner would not be relevant to claims containing definite limitations (Decision, p. 9). The Board may decide to reconsider the rejection under 35 USC § 103(a) in light of appellant's arguments with regard to the definiteness of claims 17, 26-31, and 33-37.

IV. Argument

A. 35 U.S.C. § 112 REJECTIONS

Claims 17, 26-31 and 33-37 stand rejected under 35 USC § 112, second paragraph, as allegedly being indefinite, the Examiner's Answer stating that use of the trademark, PENTIUM®, as a claim limitation renders the claim indefinite. The Examiner contends that there are at least ten different processors produced by Intel corporation that carry the trademark PENTIUM but that also contain slightly different instruction sets (Answer, p. 6).

The Board sustained the examiner's rejection, stating that if the meaning of PENTIUM or a "PENTIUM microprocessor instruction set" is subject to change, those who would endeavor, in future enterprise, to approach the area circumscribed by the claims, would not have adequate notice of the metes and bounds of the claimed subject matter. The Board argues that if the recitation of a "PENTIUM microprocessor instruction set" does not identify one and only one material or product, the recitation has no fixed and definite meaning. By way of illustration, the Board posed the following hypothetical situation: "What if Intel employs its trademark PENTIUM to describe an entirely different type of microprocessor in the future? Will the instant claims cover that possibility? If so, what kind of adequate notice would one have as to what the instant claim language covers now and/or in the future?" (Decision, pp. 5-6).

Appellant respectfully submits that the Board is in error for construing the instant claim language according to a hypothetical future meaning. Accordingly, there is good cause for the appellant to present new arguments based upon relevant decisions of the

Federal Circuit in order to demonstrate such erroneous construction.

The parent (Ser. No. 09/052,904) of the present application was filed on March 31, 1998. The Federal Circuit makes it clear that the ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application.

It was explained recently in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313; 75 U.S.P.Q.2D (BNA) 1321 (Fed. Cir. 2005): "Importantly, the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification. This court explained that point well in *Multiform Desiccants, Inc. v. Medzam, Ltd., 133 F.3d 1473, 1477 (Fed. Cir. 1998)*:

> It is the person of ordinary skill in the field of the invention through whose eyes the claims are construed. Such person is deemed to read the words used in the patent documents with an understanding of their meaning in the field, and to have knowledge of any special meaning and usage in the field. The inventor's words that are used to describe the invention--the inventor's lexicography--must be understood and interpreted by the court as they would be understood and interpreted by a person in that field [**25] of technology. Thus the court starts the decision making process by reviewing the same resources as would that person, viz., the patent specification and the prosecution history.

See also *Medrad, Inc. v. MRI Devices Corp.*, 401 F.3d 1313, 1319 (Fed. Cir. 2005) ("We cannot look at the ordinary meaning of the term . . . in a vacuum. Rather, we must look at the ordinary meaning in the context of the written description and the prosecution history."); *V-Formation, Inc. v. Benetton Group SpA*, 401 F.3d 1307, 1310 (Fed. Cir. 2005) (intrinsic record "usually provides the technological and temporal context to enable the court to ascertain the meaning of the claim to one of ordinary skill in

the art at the time of the invention"); *Unitherm Food Sys., Inc. v. Swift-Eckrich, Inc.*, 375 F.3d 1341, 1351."

See also *Research Plastics, Inc. v. Fed. Packaging Corp.*, 421 F.3d 1290, 1295 (Fed. Cir. 2005) ("Claim construction begins with the language of the claims. *Vitronics Corp. v. Conceptronic Inc.*, 90 F.ed 1576, 1582 (Fed. Cir. 1996). The words of a claim are generally to be accorded their "ordinary and customary meaning," id. at 1582, which is "the meaning that term would have to a person of ordinary skill in the art in question at the time of invention,") also citing *Phillips*, 2005 U.S. App. LEXIS 13954, at *22 ("It is presumed that the person of ordinary skill in the art read the claim in the context of the entire patent, including the specification, not confining his understanding to the claim at issue.").

Therefore, the temporal context for construction of a term is not arbitrary or hypothetical but fixed at the time of the invention. Further, absent other legal rules of construction, the ordinary meaning of the inventor's words must be the same meaning that a skilled artisan would perceive that the inventor intended, within the temporal context for construction, and upon reading the written description and the prosecution history.

In particular, the written description of the present application includes (p. 7, line 6 through p. 8, line 10, emphasis supplied) the following:

> The invention takes advantage of circuitry used to perform other single instruction multiple data (SIMD) operations such that only a relatively small amount of additional circuitry is needed to provide the PSAD instruction. In one embodiment, the PSAD instruction is implemented using two operations to generate a packed data having multiple absolute differences and an operation to sum the multiple absolute differences in the packed data to produce a PSAD.

One aspect of the invention is the use of the circuitry for a SIMD add operation to generate a packed data having multiple absolute differences by using each one of a set of sign bits to independently select the add or subtract operation for the corresponding packed data element having multiple differences. In one embodiment, when a sign bit indicates the difference in the corresponding packed data element is negative, the packed data element is subtracted from zero to produce the absolute value of the difference. When the sign bit indicates the difference in the corresponding packed data element is non-negative, the packed data element is added to zero to produce the absolute value of the difference.

Another aspect of the invention is the use of circuitry for a SIMD multiply or multiply-add, for example, to produce a sum of the packed data elements of a packed data by inserting the packed data elements into an adder tree that is used to sum the partial products in the SIMD multiply or SIMD multiply-add. In one embodiment, the packed data has packed data elements that are absolute differences. However, packed data elements containing other values may be summed using this method and apparatus.

In one embodiment, these two aspects of the invention are combined to produce a PSAD instruction. Alternatively, each aspect of the invention may be used independently with other instructions to perform the PSAD instruction.

In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the described invention. Some of these specific details may not be required to practice the invention. In other instances, well-known structures, interfaces and processes have not been shown in detail in order to avoid obscuring the described invention.

The written description of the present application also includes (p. 9, line 14 through p. 10, line 10, emphasis supplied) the following:

The decode unit 140 is shown including a packed data instruction set 145 for performing operations on packed data. In one embodiment, the packed data instruction set 145 includes a PMAD instruction(s) 150, a PADD instruction(s) 151, a packed subtract instruction(s) (PSUB) 152, a packed subtract with saturate instruction(s) (PSUBS) 153, a packed maximum instruction(s) (PMAX) 154, a packed minimum instruction(s) (PMIN) 155 and a packed sum of absolute differences instruction(s) (PSAD) 160. The operation of each of these instructions is further described herein. In one embodiment of the invention, the processor 105 supports the Pentium® microprocessor instruction set and the packed data instruction set 145. By including the packed data instruction set 145 into a standard microprocessor instruction set, such as the Pentium® microprocessor instruction set, packed data instructions can be easily incorporated into existing software (previously written for the standard microprocessor instruction set). Thus, many multimedia applications

may be executed more efficiently by using the full width of a processor's data bus for performing operations on packed data. This eliminates the need to transfer smaller units of data across the processor's data bus to perform one or more operations one data element at a time. Other standard instruction sets, such as the PowerPC™ and the Alpha™ processor instruction sets may also be used in accordance with the described invention. (Pentium® is a registered trademark of Intel Corporation. PowerPC™ is a trademark of IBM, APPLE COMPUTER, and MOTOROLA. Alpha™ is a trademark of Digital Equipment Corporation.) Alternative embodiments of the invention may contain more or less, as well as different, packed data instructions and still utilize the teachings of the invention.

Appellant respectfully submits that in accordance with the disclosure of the written description, one of ordinary skill in the art of microprocessor design and manufacture, presumably a competitor capable of making a processor to execute the PENTIUM microprocessor instruction set as well as another packed data instruction set, would understand the inventor's intent to take a processor having a standard microprocessor instruction set, such as the PENTIUM microprocessor instruction set, including a packed data instruction set and to use disclosed aspects of the invention to produce a PSAD instruction. Since no rejection was made under the first paragraph of 35 USC § 112, a skilled artisan presumably would not be confused as to what was required at the time to design and manufacture a processor having a standard microprocessor instruction set, such as the PENTIUM microprocessor instruction set.

As of the filing date, March 31, 1998, the processors produced by Intel corporation that carried the trademark PENTIUM included the original PENTIUM Processor (introduced March 22, 1993), the PENTIUM Pro Processor (introduced November 1, 1995; which included conditional move instructions, FXRSTOR, FXSAVE and system enter/exit instructions), the PENTIUM Processor with MMX™ Technology (MMX Technology was publicly released March 5, 1996) and the PENTIUM II Processor

(introduced May 7, 1997). All four processor types executed the original PENTIUM Processor instruction set, and all but the original PENTIUM Processor also executed the additional PENTIUM Pro instructions. The latter two executed all PENTIUM Pro instructions as well as the packed data instructions of MMX Technology.

Such practice of sequentially introduced processor families executing a superset of preceding processors is well understood by those of skill in the art of microprocessor design and manufacture and is referred to in the art as "backwards compatibility." Appellant respectfully submits that a skilled artisan at the time would have had access to and would have had an understanding of such technical details and practices in accordance with his understanding of the disclosure of the written description. Thus, appellant respectfully submits that when correctly construed through the eyes of a skilled artisan with an understanding of the written description at the time of the invention, the limitations, "a decode unit to decode...," and "a processor to execute instructions of the PENTIUM microprocessor instruction set," as set forth, respectively, in claims 17 and 26, do provide adequate notice of the metes and bounds of the claimed subject matter.

The Supreme Court held, in *Carnegie Steel Co. v. Cambria Iron Co.*, 185 U.S. 403, 437, that (parenthetical interpretation inserted by appellant): "The specification of the patent is not addressed to lawyers, or even to the public generally, but to the manufacturers of steel (i.e. to those of skill in the relevant art), and any description which is sufficient to apprise them in the language of the art of the definite feature of the invention, and to serve as a warning to others of what the patent claims as a monopoly, is sufficiently definite to sustain the patent. He may assume that what was already known in the art of manufacturing steel was known to them, and, as observed by Mr. Justice

Bradley, in *Webster Loom Co. v. Higgins*, 105 U.S. 580, 586, "He may begin at the point where his invention begins, and describe what he has made, that is new, and what it replaces of the old. That which is common and well known is as if it were written out in the patent and delineated in the drawings." "

Therefore, appellant respectfully submits for the Board's reconsideration, that the language set forth in claims 17 and 26 provide adequate notice of metes and bounds in the language of the art, and serve as a warning to others of what appellant claims, taking a processor having the PENTIUM microprocessor instruction set and operations on packed data and initiating a first set of the operations on packed data responsive to decoding a PSAD instruction.

It is not necessary that "the PENTIUM microprocessor instruction set," have one and only one meaning as suggested in the Board's opinion (Decision, p.5). Rarely does any language term or phrase have one and only one meaning. Nor is it necessary that skilled artisans would all agree upon the ordinary meaning that the inventor intended. Appellant respectfully submits that a claim is not indefinite simply because it covers a number of possible embodiments.

The Court of Customs & Patent Appeals in considering the expression "organic and inorganic acids," which was alleged to be indefinite and of uncertain scope, held that, "Although there are undoubtedly a large number of acids which come within the scope of 'organic and inorganic acids,' the expression is not for that reason indefinite." *In re Skoll*, 187 USPQ 481 (CCPA 1975).

It is enough that appellant point out and define the metes and bounds of the subject matter that is regarded as their invention and will be protected by the patent grant

with a reasonable degree of clarity and particularity.

Appellant has shown that the PENTIUM microprocessor instruction set was known to persons skilled in the art, and was readily obtainable at the time the application was filed. Thus, the trademark, PENTUIM, is descriptive of the source of a well known, publicly disclosed, microprocessor instruction set, which had a fixed and definite meaning at the time of the invention and which is not a particular product but rather a highly specified programming interface for numerous computers, device drivers, operating systems and compilers around the world.

Appellant respectfully submits that without properly attempting a construction of the ordinary meaning of "the PENTIUM microprocessor instruction set," the rejection of claims 17 and 26 for use of the trademark, PENTIUM, is effectively a rejection for use of a trademark, per se. Yet, according to MPEP 2173.05(u), a trademark in a claim is not, per se, improper under 35 USC § 112, second paragraph.

As the appellant has explained in detail (Brief, p. 12, lines 9-21 and p. 14, line 5 through p. 15, line 6), the phrase, "instructions of the PENTIUM microprocessor instruction set," had a fixed and definite meaning as a well established *de facto* standard of compatibility, and would, therefore, apprise one skilled in the art of claims 17 and 26's respective scope.

Accordingly, appellant submits that Claims 17 and 26 set out and circumscribe the claimed subject matter with a sufficient degree of precision and particularity. In light of the argument presented above, appellant respectfully submits that claims 17 and 26-38 are in compliance with 35 USC § 112, second paragraph.

B. 35 U.S.C. § 103(a) REJECTIONS

The Board summarily reversed the rejection of claims 17, **26**-31, and 33-37 based on 35 USC § 103(a) as allegedly being unpatentable over US Patent 5,859,789 (hereafter "Sidwell") in view of Visual Instruction Set (VIS ™) User's Guide, Sun Microsystems, March 1997 (hereafter "Sun"). The article by Ruby Lee, titled "Subword Parallelism with MAX-2," IEEE Micro, pp. 51-59, August, 1996 (hereafter "Lee(2)") was also cited by the Examiner as extrinsic evidence of the general knowledge of one skilled in the art (Answer, p. 7).

The Board indicated that their technical reversal did not imply that the art relied upon by the Examiner would not be relevant to claims containing definite limitations (Decision, p. 9). In light of the arguments presented above with regard to the definiteness of claims 17, 26-31, and 33-37, the Board may decide to reconsider the rejection of claims 17, 26-31, and 33-37 under 35 USC § 103(a). Accordingly, appellant believes there is good cause to provide the following arguments for rehearing.

With regard to Claims 17 and **26**-29 the Examiner's Answer maintained that it would have been obvious to combine Sun's packed sum of absolute differences to Sidwell's system because Sidwell taught that the packed arithmetic unit performed additional operations (col. 5, lines 15-22) and Sun taught that a packed sum of absolute differences instruction was beneficial in accelerating motion compensation to support real-time video compression (p. 88).

The Examiner's Answer also introduced Lee(2) as evidence that packed data operations such as that disclosed by Sidwell were known within the general knowledge of

one skilled in the art to be useful for performing media processing, such as video processing. Appellant respectfully notes that Lee(2) does not, however, provide a suggestion for making the combined system of Sidwell and Sun compatible with the PENTIUM® microprocessor instruction set.

The Examiner's Answer maintained that it would have been obvious to make a combined system of Sidwell and Sun compatible with the PENTIUM microprocessor instruction set because the PENTIUM microprocessor instruction set was the most widely used microprocessor instruction set in the world and the system would have been immediately compatible to the widest variety of available programs.

The multiply-add instruction of Sidwell (muladd2ps) employs three operands (e.g. see Sidwell, col. 8, lines 24 and 34-37). The vis_pdist() instruction of Sun also requires three operands one of which is both a source and a destination (e.g. see Sun, p. 88, line 10).

The appellant has argued that one difference between the claimed decoder of instructions of the PENTIUM microprocessor instruction set and the expected properties of the combined system of Sidwell and Sun is the absence of an expected third operand to make the combined system of Sidwell and Sun, perform Sun's vis_pdist() instruction, compatible with the PENTIUM® microprocessor instruction set, which has a well known opcode format permiting two operands, one of the operands acting both as a source operand and a destination operand.

The Board states that appellant's arguments are not persuasive as they relate to features not appearing in the claims and that they find it hard to base patentability on what is "absent" from a claim (Decision, p. 9).

Appellant respectfully submits that the Board has not attempted a construction of the ordinary meaning of "the PENTIUM microprocessor instruction set," through the eyes of a skilled artisan with an understanding of the written description at the time of the invention. Since the PENTIUM microprocessor instruction set was, as the Examiner asserts, "the most widely used microprocessor instruction set in the world," and since it was frequently copied by competitors having skill in the art of designing and manufacturing processors, much was known to a skilled artisan about the PENTIUM microprocessor instruction set, including of course the inherent features of its instruction format(s).

If the Examiner's proposed modification to make a combined system of Sidwell and Sun compatible with the PENTIUM microprocessor instruction set changes the principal of operation of a reference, for example, by computing the claimed sum of absolute differences of a first identified set of packed data rather than an accumulation of current absolute differences and prior absolute differences of unidentified packed data, then the references are not sufficient to render the claims *prima facie* obvious (See MPEP 2143.01, last three paragraphs).

To decode and execute the vis_pdist() instruction of Sun having three source operands in a processor for executing two-operand instructions of the PENTIUM microprocessor instruction set is not suggested by any of the cited references.

The Examiner (Answer, p. 20 and p. 22) and the Board (Decision, p. 9) are in error for misinterpreting the appellant's argument as to assert, merely, that a particular limitation was not taught or suggested by the cited reference. Certainly, it is established that making the combined system of Sidwell and Sun compatible with the PENTIUM

microprocessor instruction set is not taught or suggested by the cited references.

Appellant is further rebutting an obviousness assertion, where the Examiner is, based on common knowledge and without support of documentary evidence, asserting that it would have been obvious to make a combined system of Sidwell and Sun compatible with the PENTIUM microprocessor instruction set (e.g. Answer, p. 9, last par.). The Examiner is in effect taking "official notice" of common knowledge in the art (See MPEP 2144.03). Thus such common knowledge must necessarily include enough detailed general knowledge of what is technically required to make a combined system of Sidwell and Sun compatible with the PENTIUM microprocessor instruction set. Wherein the Examiner relies upon common knowledge in the art to establish his alleged *prima facie* case of obviousnes , it is not improper for appellant to rely upon that common knowledge to rebut the Examiner's alleged *prima facie* case.

Appellant is arguing that the Examiner's reliance upon common knowledge of the PENTIUM microprocessor instruction set by one skilled in the art while omitting specific details within that general knowledge of one skilled in the art is improper when such detailed general knowledge would suggest a difference between the claimed decoder of the PENTIUM microprocessor instruction set and the expected properties of the combined system of Sidwell and Sun. Thus, the appellant has reached a different conclusion than the Examiner, that making the combined system of Sidwell and Sun compatible with the PENTIUM microprocessor instruction set would not be obvious from the cited references in light of such detailed general knowledge in the art.

The Examiner (Answer, p. 20, last par.; p.22, par. 2-3; p. 23, par. 2; and p. 24, par. 2-3) is further in error for suggesting that Sun's system naturally suggests a two operand

format. As the appellant has stated in the Appeal Brief, the vis_pdist() instruction of Sun, has a three operand format, one of which is both a source and also a destination (Sun, p. 87, 4.7.11, Syntax and Description).

Sun clearly states, "vis_pdist() takes three double precision arguments *pixel1*, *pixel2* and *accum*." Sun further points out that. "*pixel1* and *pixel2* contain 8 pixels each... the destination register [*accum*] is a double-precision floating point register which contains an integral value."

The Examiner's Answer mischaracterizes the appellants arguments as counting operands in two different ways (Answer, p. 23, line 1) and quotes from Sun, p. 88, where it states (Answer, p. 23, par. 2; emphasis supplied by the Examiner) "To use vis_pdist() from C, it is **necessary** for the accumulating register *accumulator* to appear both as an argument and as the receiver of the return value." But the Examiner's argument is misleading because the Examiner fails to include the example of C code directly below the quoted statement in Sun, which includes the following line:

"`accum = vis_pdist(pixel1, pixel2, accum);`".

Clearly, the appellant is not miscounting the three source arguments in parenthesis, and clearly the necessity in C that *accum* must also appear to the left of the equal sign to receive the return value does not in any way alter the vis_pdist() instruction to suggest a two operand format as was suggested by the Examiner's Answer.

The Examiner's Answer further includes additional arguments[1,2], some of which

[1] The Examiner's Answer (p.21, par. 9; & p. 22, par. 2) addresses the appellants assertion that the IMUL instructions with an implicit operand are still effectively two operand instructions, by pointing out that there is an IMUL instruction, which also permits an immediate operand, concluding three operands are possible. The Examiner's Answer then fails to proffer a modified conclusion that it would have been obvious to one of skill in the art to use an immediate operand as one of the three operands required by Sun's vis_pdist()

the appellant respectfully submits are red herrings and can only serve to distract from the real question at issue. Can making a combined system of Sidwell and Sun compatible with the PENTIUM microprocessor instruction set be considered obvious when it requires modifications that would cause the modified system to no longer perform the operation defined by the vis_pdist() instruction of Sun?

The appellant concludes (in accordance with MPEP 2143.01) that, especially when no such modification is suggested by any of the references, such action should not be considered obvious.

Accordingly in light of the above arguments, Claims 17, 26-31, and 33-37 are not obvious in view of the cited references.

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instruction as the Examiner has previously argued with regard to an implicit operand. The appellant respectfully submits that such a conclusion would necessarily be incorrect since an immediate operand is a constant value, determined at compilation time, and therefore, would cause the modified system to no longer perform the operation defined by Sun's vis_pdist() instruction as it's intended use is to compress video data which is not constant or predetermined at the time the compression program is compiled (see MPEP 2143.01, last par.).

[2] The Examiner's Answer (p.21, par. 1-8; p. 23, par. 3-5, p. 24, par. 1; and p. 25, par. 2-5) mischaracterizes the appellants arguments as asserting that a particular unclaimed limitation was not taught or suggested by the cited references. Rather, the appellant has respectively asserted in the Appeal Brief **(p. 20, par. 3 through p. 21, par. 1; in accordance with MPEP 716.02)** that to decode and execute the vis_pdist() instruction of Sun having three source operands in a processor for executing the PENTIUM microprocessor instruction set as claimed is not suggested by the cited references, and that based on the prior art disclosures the use of the PENTIUM microprocessor instruction set having the known property of a two-operand format would be unexpected and unobvious and of both statistical and practical significance; **(p. 22, par. 2-3; in accordance with MPEP 2143.01, last 3 pars., and 716.02)** that where the suggestion to make the combined system of Sidwell and Sun, perform Sun's vis_pdist() instruction compatible with the PENTIUM microprocessor instruction set is not suggested by the cited references, and after making such modification the combination would no longer perform the operation defined by Sun's vis_pdist() instruction, such modification is unobvious; **(p. 21, par. 2 through p. 23 par. 2; in accordance with MPEP 2143.01, last 3 pars., 2141.02, last par., and 716.02)** that despite the Examiner's assertion in the Office Action (8.5) of the obviousness of using implicit operands as in the IMUL instruction of the PENTIUM microprocessor instruction set for the combined system of Sidwell and Sun to perform Sun's vis_pdist() instruction, the appellant maintains that where no suggestion of such modification is provided either by the cited references or by a common knowledge of IMUL in one of ordinary skill in the art, where Sun's vis_pdist() requires three source operands and the IMUL instruction with implicit operands is still a two-operand instruction, where Sun teaches away from the IMUL technique of employing an implicit source that is also the destination, and where an implicit operand which a claimed invention would have been expected to possess based on the teachings of the cited art is absent, the combination is unobvious.

Conclusion

Appellant submits that all claims now pending are in condition for allowance. Such action is earnestly solicited at the earliest possible date. If there is a deficiency in fees, please charge our Deposit Acct. No. 02-2666.

Respectfully submitted,

Date: 8-13-2006

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V. Claims Appendix: Claims Allowed and Involved in Appeal (Clean Copy)

1-15. (Cancelled)

16. (Previously Presented) A processor comprising:

a decode unit to decode a plurality of packed data instructions including a packed sum of absolute differences (PSAD) instruction having a first format to identify a first set of packed data, and a packed multiply-add (PMAD) instruction having a second format to identify a second set of packed data, said decode unit to initiate a first set of operations on the first set of packed data responsive to decoding the PSAD instruction and to initiate a second set of operations on the second set of packed data responsive to decoding the PMAD instruction; and

an execution unit to perform a first operation of the first set of operations initiated by the decode unit and to perform a second operation of the second set of operations initiated by the decode unit.

17. (Previously Presented) The processor of Claim 16, wherein the decode unit further decodes a plurality of instructions of a PENTIUM microprocessor instruction set.

18. (Previously Presented) The processor of Claim 16, wherein the first set of operations comprises:

a packed subtract and write carry (PSBWC) operation;

a packed absolute value and read carry (PABSRC) operation; and

a packed add horizontal (PADDH) operation.

19-20. (Cancelled)

21. (Previously Presented) The processor of Claim 16, wherein performing the first operation causes the execution unit to:

produce a first plurality of partial products in a multiplier having a plurality of partial product selectors;

insert an element of a first plurality of elements of a first packed data into and substituting for bit positions of one or more of the first plurality of partial products by using partial product selectors corresponding to the bit positions; and

add the first plurality of elements together to produce a first result including a field comprising a sum of the first plurality of elements, said field having a least significant bit.

22. (Previously Presented) The processor of Claim 21, wherein performing the first operation further causes the execution unit to:

shift the first result to produce a second result having a least significant bit position and to align the least significant bit of the field with the least significant bit position of the second result.

23. (Previously Presented) A processor comprising:

a decode unit to decode a plurality of packed data instructions including a packed sum of absolute differences (PSAD) instruction having a first format to identify a first set of packed data, and a packed multiply-add (PMAD) instruction having a second format to identify a second set of packed data, said decode unit to initiate a first set of operations on the first set of packed data responsive to decoding the PSAD instruction and to initiate a second set of operations on the second set of packed data responsive to decoding the PMAD instruction; and

an execution unit to perform a first operation of the first set of operations initiated by the decode unit and to perform a second operation of the second set of operations initiated by the decode unit;

wherein performing the first operation causes the execution unit to:

produce a first plurality of partial products in a multiplier having a plurality of

partial product selectors,

insert an element of a first plurality of elements of a first packed data into and substituting for bit positions of one or more of the first plurality of partial products by using partial product selectors corresponding to the bit positions, and

add the first plurality of elements together to produce a first result including a field comprising a sum of the first plurality of elements, said field having a least significant bit;

and wherein performing the second operation causes the execution unit to:

produce a second plurality of partial products in the multiplier having the plurality of partial product selectors, the second plurality of partial products comprising four distinct sets of partial products including a first set of partial products corresponding to a first product for elements of the second set of packed data, a second set of partial products corresponding to a second product for elements of the second set of packed data, a third set of partial products corresponding to a third product for elements of the second set of packed data, and a fourth set of partial products corresponding to a fourth product for elements of the second set of packed data; and

add the first set of partial products together with the second set of partial products to produce a first distinct element of a packed result and add the third set of partial products together with the fourth set of partial products to produce a second distinct element of the packed result.

24. (Previously Presented) The processor of Claim 23, wherein the second format identifies the second set of packed data as packed words.

25. (Cancelled)

26. (Previously Presented) A processor to execute instructions of the PENTIUM microprocessor instruction set, the processor comprising:

decode logic to decode a packed sum of absolute differences (PSAD) instruction having a first format to identify a first set of packed data, said decode logic to initiate a

first set of operations on the first set of packed data responsive to decoding the PSAD instruction;

execution logic to perform a first operation of the first set of operations initiated by the decode logic; and

a bus to provide the first set of packed data to the execution logic for performing of the first operation.

27. (Previously Presented) The processor of Claim 26, wherein the decode logic comprises a look-up table.

28. (Previously Presented) The processor of Claim 26, wherein the decode logic comprises integrated circuitry.

29. (Previously Presented) The processor of Claim 28, wherein the decode logic further comprises executable operations.

30. (Previously Presented) The processor of Claim 29, wherein the decode logic comprises:

a packed subtract and write carry (PSBWC) operation;

a packed absolute value and read carry (PABSRC) operation; and

a packed add horizontal (PADDH) operation.

31. (Previously Presented) The processor of Claim 26, wherein the first format identifies the first set of packed data as packed bytes.

32. (Cancelled)

33. (Previously Presented) The processor of Claim 26, wherein performing the first operation causes the execution logic to:

produce a first plurality of partial products in a multiplier having a plurality of

partial product selectors;

insert an element of a first plurality of elements of a first packed data into and substituting for bit positions of one or more of the first plurality of partial products by using partial product selectors corresponding to the bit positions; and

add the first plurality of elements together to produce a first result including a field comprising a sum of the first plurality of elements, said field having a least significant bit.

34. (Previously Presented) The processor of Claim 33, wherein performing the first operation further causes the execution logic to:

shift the first result to produce a second result having a least significant bit position and to align the least significant bit of the field with the least significant bit position of the second result.

35. (Previously Presented) The processor of Claim 26, the decode unit to decode a packed multiply-add (PMAD) instruction having a second format to identify a second set of packed data, said decode unit to initiate a second set of operations on the second set of packed data responsive to decoding the PMAD instruction.

36. (Previously Presented) The processor of Claim 35, execution unit to perform a second operation of the second set of operations initiated by the decode unit.

37. (Previously Presented) The processor of Claim 35, wherein the second format identifies the second set of packed data as packed words.

38. (Cancelled)

39. (Previously Presented) A processor comprising:

decode logic to decode a packed sum of absolute differences (PSAD) instruction having a first format to identify a first set of packed data, said decode logic to initiate a

first set of operations on the first set of packed data responsive to decoding the PSAD instruction, the first set of operations comprising:

a packed subtract and write carry (PSUBWC) operation;

a packed absolute value and read carry (PABSRC) operation; and

a packed add horizontal (PADDH) operation.; and

execution logic to perform the first set of operations initiated by the decode logic.

40. (Previously Presented) The processor of Claim 39, wherein the first format identifies the first set of packed data as packed bytes.

41. (Previously Presented) The processor of Claim 39, wherein performing the PSUBWC operation causes the execution logic to:

subtract one of a plurality of elements of a first packed data of the first set of packed data from a corresponding one of a plurality of elements of a second packed data of the first set of packed data to produce a first result having a plurality of difference elements and a plurality of sign indicators; and

store the plurality of difference elements and the plurality of sign indicators.

42. (Previously Presented) The processor of Claim 39, wherein performing the PABSRC operation causes the execution logic to:

receive a plurality of difference elements and a plurality of sign indicators;

produce a result data having a plurality of absolute value elements, each absolute value element produced by

(a) subtracting one of the plurality of difference elements from a corresponding constant value if the sign indicator corresponding to that element is in a first state, or

(b) adding one of the plurality of difference elements to a corresponding constant value if the sign indicator corresponding to that element is in a second state.

43. (Previously Presented) The processor of Claim 39, wherein performing the PADDH operation causes the execution logic to:

produce a first plurality of partial products in a multiplier having a plurality of partial product selectors;

insert an element of a first plurality of elements of a first packed data into and substituting for bit positions of one or more of the first plurality of partial products by using partial product selectors corresponding to the bit positions; and

add the first plurality of elements together to produce a first result including a field comprising a sum of the first plurality of elements, said field having a least significant bit.

44. (Previously Presented) The processor of Claim 43, wherein performing the PADDH operation further causes the execution logic to:

shift the first result to produce a second result having a least significant bit position and to align the least significant bit of the field with the least significant bit position of the second result.

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